(12) UK Patent Application (19) GB (11) 2 077 008 A

(21) Application No 8016704
(22) Date of filing
21 May 1980
(43) Application published
9 Dec 1981
(51) INT CL³ G06F 7/38
(52) Domestic classification
G4A AR
(56) Documents cited
GB 1543852
GB 1543515
GB 1353213
(58) Field of search
G4A
G4H
(71) Applicant
Dr Jiri Slechta AFIMA
MInstP
18 Lidgett Hill
Leeds 8
LS8 1PE
(72) Inventor
Dr Jiri Slechta AFIMA
MInstP

(54) On how to achieve mathematical convergency in digital computers

(57) The invention achieves the ideal unbiased computing with preset precision by introducing a non-causal "round-off" procedure into the arithmetic units of digital computers which modifies the content of the last bit of the digital word in the arithmetic unit according to the content of the auxiliary bit which is the next one to the last bit from the right-hand side and the output of the generator of a simulated "coin tossing" built into the arithmetic units. The generator should be of a numerical nature of an integer character. There is presented one possible realization of such a generator in the form of "Digital unbiased ideal random binary switch (0, 1)".

The invention can be exploited in all types of digital computers, including card programmable calculators.

GB 2 077 008 A

SPECIFICATION

On how to achieve mathematical convergency in digital computers

Technical Field: Arithmetic Units of Digital Computers.

Background Art: When using all the digital computers available at the present time there is often the case that algorithms which are proven, by the techniques of Mathematical Analysis or Abstract Numerical Mathematics, to converge do not do so really numerically on these computers. Examples of that to happen are given in the book "Numerical Processes in Differential Equations" by J. Babuska, J. Prager and E. Vitasek (John Wiley & Sons, New York, 1966). The reason for it is the way of how numbers are rounded off in the computers of the present design.

In the present method of the "rounding off" in the arithmetic unit of those computers there is available one auxiliary digit in addition to what is maximally displayed. If the value of that auxiliary digit is ≤ 5 (or < 5) then the previous digit is left unchanged, but if that auxiliary digit is > 5 (or ≥ 5) then the value of the previous digit is increased by one.

The main disadvantages of that method are:

a) the algebra of irracional numbers is reduced to the algebra of racional numbers, only,

b) into the computation there are introduced systematic errors which do accumulate throughout a lengthy computation.

Both these disadvantages of the present method cause the problem stated above.

Nature of the Invention: To amend the problem there is necessary to introduce the white noise-like "round off" procedure into the arithmetic unit. This means that when the auxiliary digit is equal to 5 then the previous one is either increased or decreased by one according to the output of a generator of random numbers built into the arithmetic unit.

My method stated here can be justified from the general theory of numbers.

Best mode of testing the idea of the Invention: A large computer of a common design into which there is built an arithmetic unit designed according to this my Invention.

Exploration in Industry: It can be used in models of computers or calculators of any technological realization starting from programmable calculators to large computers.

It will safe computer time as the number of digits actually used in the arithmetic units can be equal only to the number of those really displayed, this can be adjustable, plus one.

CLAIMS

1. The way of achieving the unbiased computing with preset precision by means of treating the case "equal to 5", in decimal system, in the auxiliary last bit of the arithmetic unit of digital computers according to the output of the simulated ideal "coin tossing" that is depending upon its output to increase or decrease the content of the bit preceding the auxiliary one by 1. That is called a noncausal round-off.

2. The way of how the noncausal round-off, as described in the claim 1, can be realized in the binary system that is to set the context of the auxiliary last bit to be 0 or 1 according to the output of the simulated "coin tossing".

3. Technical realizations of the noncausal round-off which are reducable to what is claimed in claims 1 and 2, in principle.

Printed for Her Majesty's Stationery Office
by Burgess & Son (Abingdon) Ltd.—1981.
Published at The Patent Office, 25 Southampton Buildings,
London, WC2A 1AY, from which copies may be obtained.